SOCRATES

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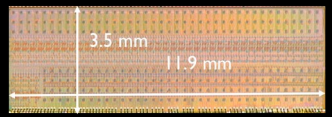
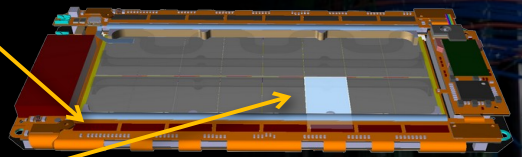
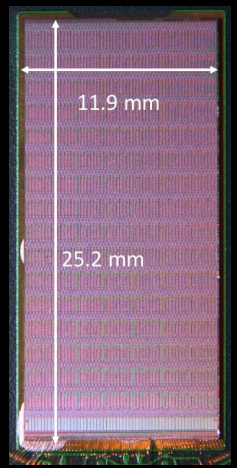
Micro-Chips for Mega-Machines

On-detector ASICs
e.g. "SSA" and "MPA"
~ 100k units

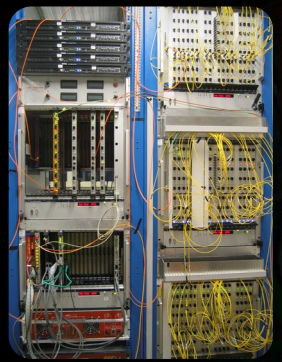


On-detector Module
e.g. "PS-Module"
~ 6k units





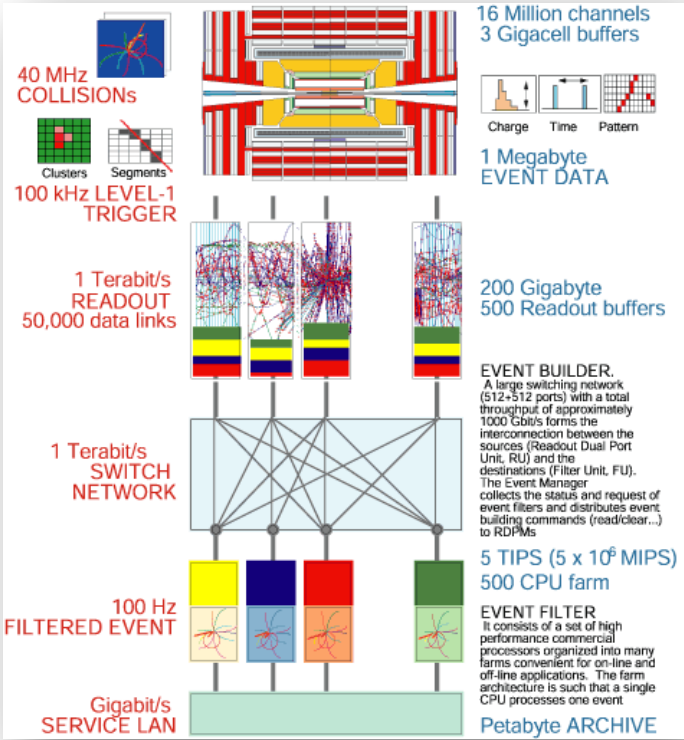
Off-detector
Electronics



CMS Experiment
at the LHC accelerator

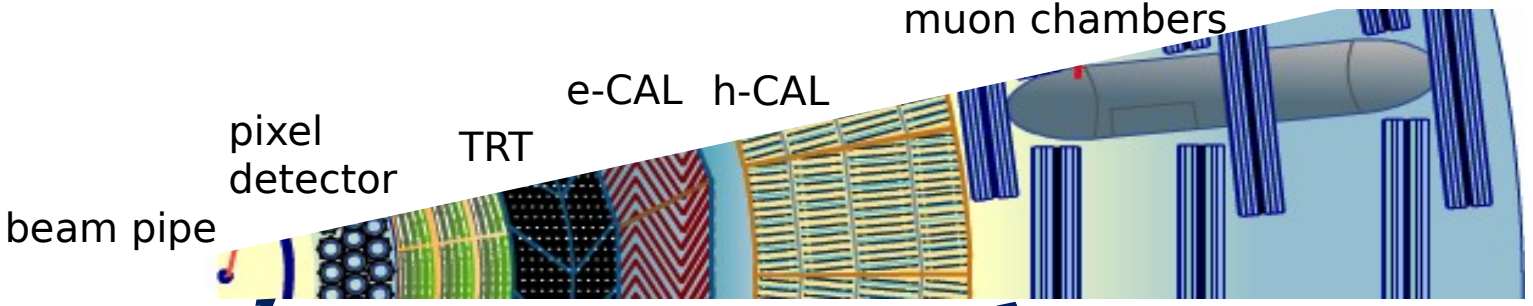
Custom Functionalities for On-detector ASICs

- **High number of readout channels**
- **High bandwidth of event data**
  - E.g., out of trillions of events only one may generate a Higgs boson!
- **Unique Signal Processing Techniques**
  - Data reduction at the source
  - Particle momentum filtering, hit-clustering, time-of-flight, etc.



CMS data readout chain

ASICs in operation of ATLAS detector

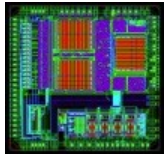


Slide by E. Heijne
ISSCC 2014

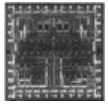
FE-I3 pix det
28 000 chips
80 M segments
1.7 m² Si sensor

ABCD Si det
50 000 chips
6 M segments
60 m² Si sensor

ASDBLR TRT det
38 000 chips

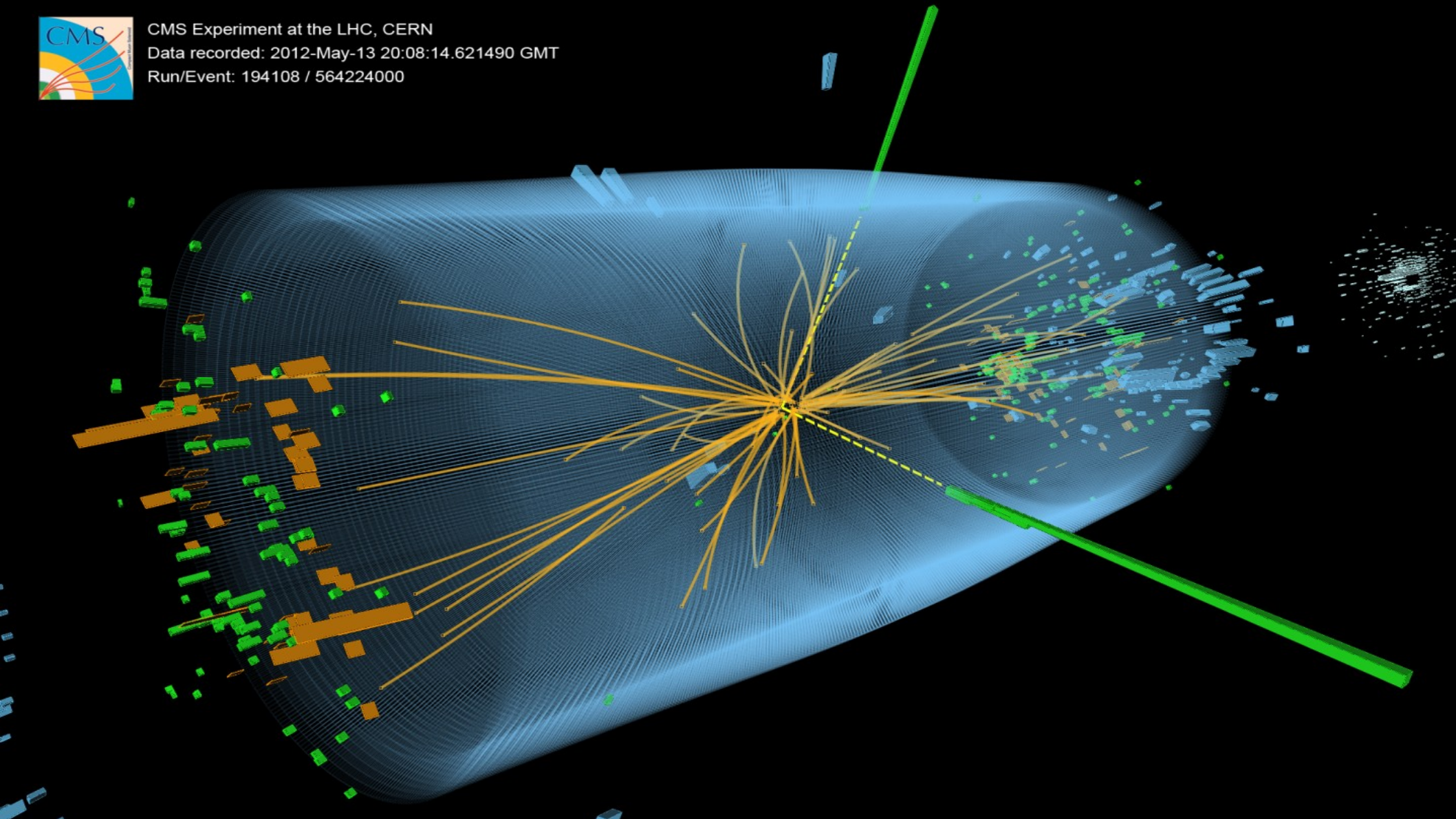


DTMROC TRT det
19 000 chips



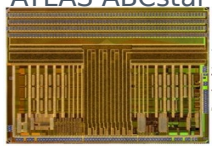
ASD muon det
148 000 chips

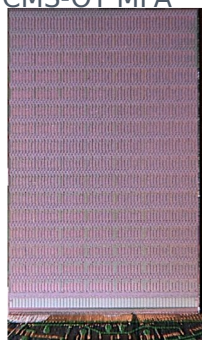
ATLAS total
~ 800k chips
Majority of which are ASICs

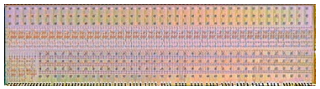

CMS Experiment at the LHC, CERN
Data recorded: 2012-May-13 20:08:14.621490 GMT
Run/Event: 194108 / 564224000

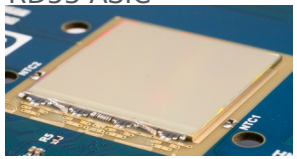
ASICs developed for next LHC Upgrades

GBT-SCA 

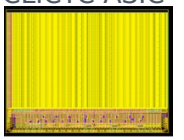
ATLAS ABCstar 

CMS-OT MPA 

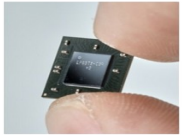
CMS-OT SSA 

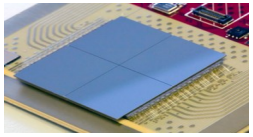
RD53 ASIC 

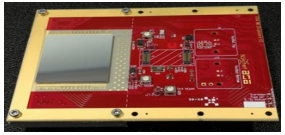
LpGBT ASIC 

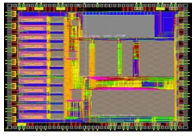
CLICTC ASIC 

DC-DC converters 

Versatile links 

MEDIPIX 

TIMEPIX 

HGCAL ECON 

67 unique chips!

Experiment | Design Name

ALICE (and NA62)	SAMPA, ALPIDE, FEERIC, Non-LHC, TDCpix (NA62)
LHCb	VELO – VeloPix, Upstream Tracker – SALT, RICH – CLARO, SciFi – PACIFIC, CALO – ICECAL, MUON - nSYNC
ATLAS	ITK Pixel, Monolithic Pixel, ITK strips, Lar Calorimeter, HGTD, Muon NSW, Muon MDT, Muon TGC, Muon RPC, Trigger-DAQ
CMS	GEM VFAT3, OT CBC, OT CIC, OT MPA, OT SSA, EB CATIA, EB LITE-DTU, IT ROC, EC Si ROC (HGCROC, H2GCROC), EC TCON, ECON, DCON, EC LDO, BTL TOFHIR, BTL ALDO2, ETL ETROC, CMS CFO
Common ASICs	lpGBT, LDQ10, lpGBTIA, GBTX, GBT-SCA, GBLD, GBTIA, FEAST2, bPOL12V, bPOL2V5, linPOL12V, RD53

Introduction

- **Costs of ASICs design**
  - Increased complexity
  - Flexibility vs Performance/Cost tradeoff
    - CPU → GPU → FPGA → ASIC

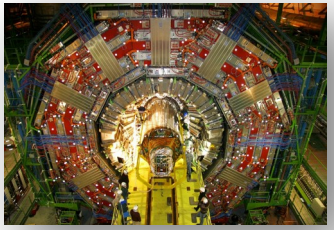
Reusable and **programmable** IPs for **system-on-chips** (SoCs)

- **Edge computing**
  - Latency, data privacy, security, energy efficiency, performance, …

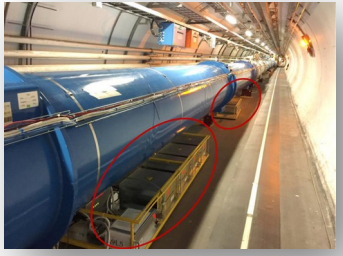
EP R&D – Intelligence on Detector (WP5.3)

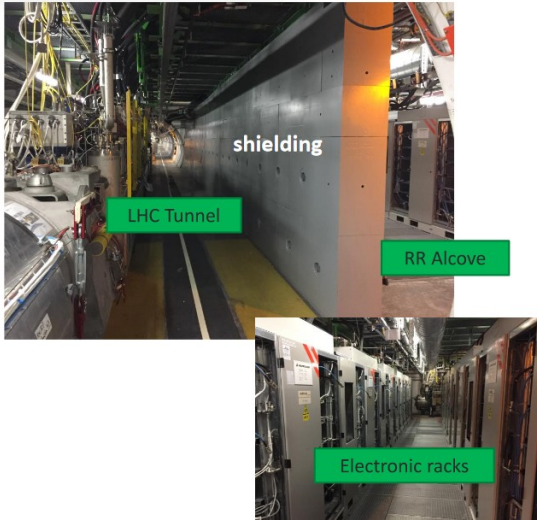
- **SoC radiation-tolerant ecosystem (SOCRATES)**
  - SoC generator (for HEP)
  - RISCV-based systems
    - Open-source
    - Mature (embedded-class)
    - Customizable / extensible
  - RIGOLETTO European p
    - Funding for tools de

High-energy physics applications

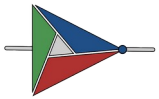


- **Control**
  - Lower calibration time for detector systems
  - Faster monitoring of beam characteristics
  - Power management, sensors monitoring, etc.
- **Data**
  - Pre-processing
    - Filtering, clustering, ...





SOCRATES (SOC RAdiation Tolerant Eco-System)



SoCMake
Build System

Radiation Hardening

DEVELOPMENT STAGE:
- ✔ Advanced
- ❑ *Early*

Hardware composition

- ✔ Generate the top-level SoC
- ✔ Integrate IP blocks
- ✔ Infer interconnects (crossbars, adapters)
- ✔ Rad-hardened blocks

Software generation

- ✔ Invoke RISC-V toolchain
- ✔ Generate hardware abstraction layer
- ✔ Generate linker scripts
- ❑ *Software fault tolerance*

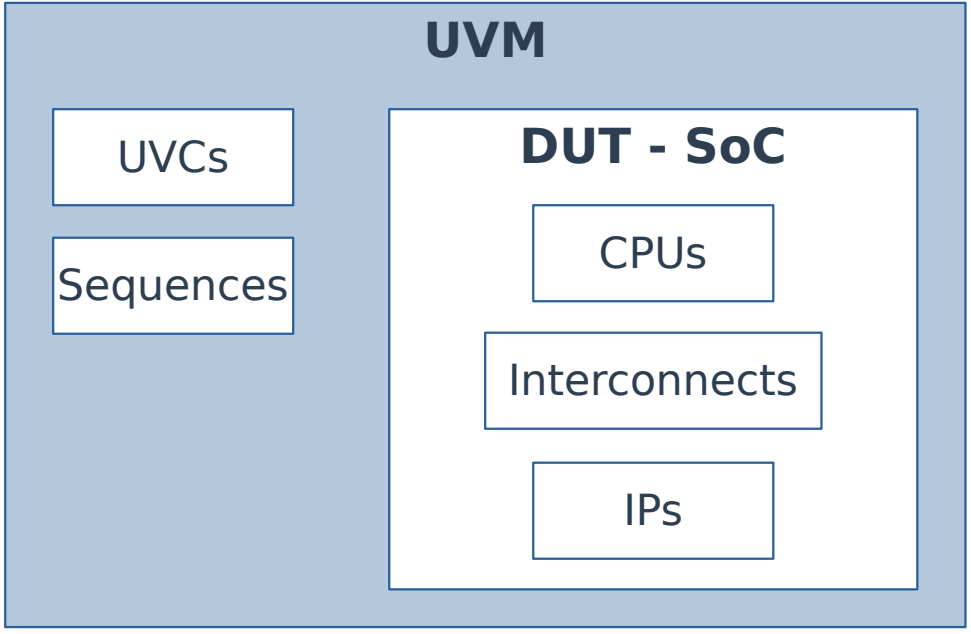
Verification environment

- ✔ Functional testing environment
- ✔ SystemC-UVM environment
- ✔ FPGA prototyping
- ✔ Fault injection framework

ASIC - SoC design

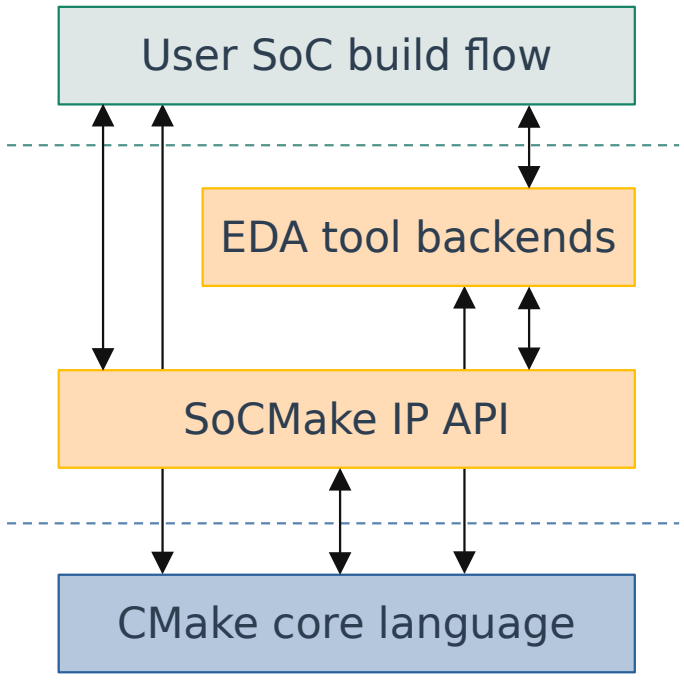
- **RTL simulation**
- **Cross-compile CPU firmware**
  - ASM, C, C++ source files
  - Third-party libraries
    - FreeRTOS, Zephyr, …
- **DPI-C simulation extensions**
- **C++ verification (UVM-SystemC)**

SW + HW compilation needed!



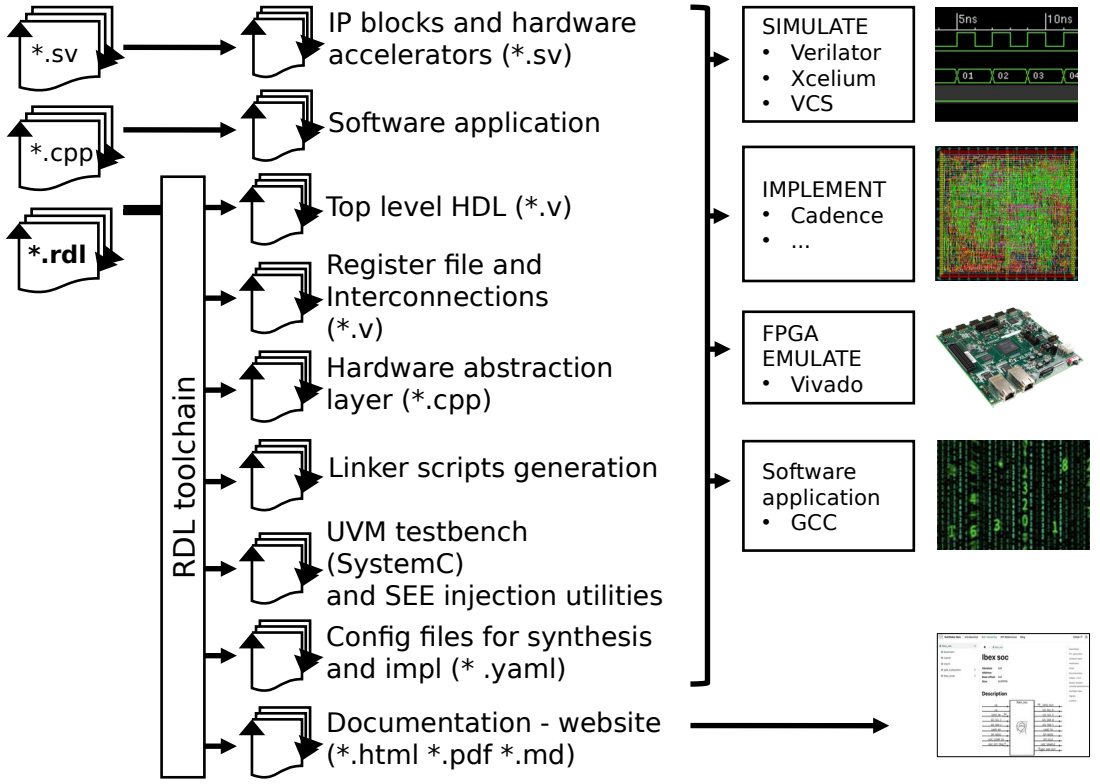
SoCMake

- **CMake**
  - First class ASM, C, C++ support
  - Scripting language
- **CMake HW extension**
  - One language to build them all

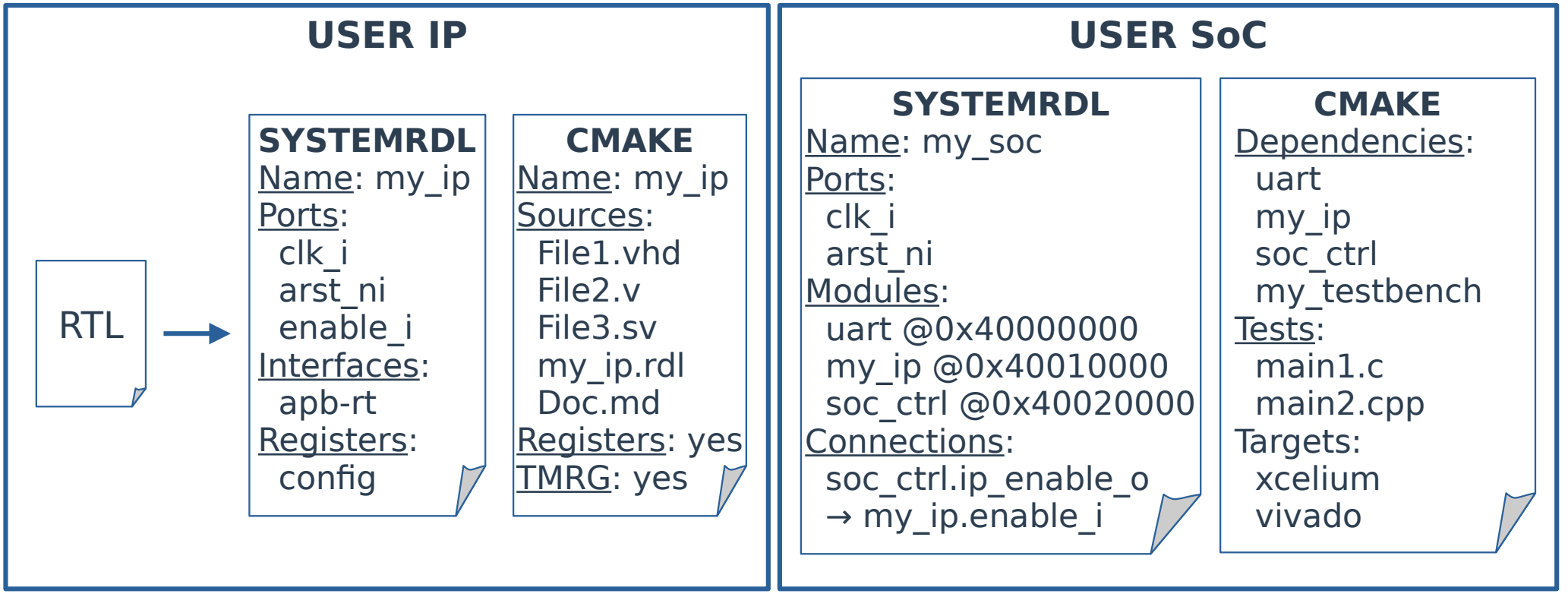


SoCMake: a HW/SW Build System

- **CMake** to generate a HW/SW build system for SoCs
- Supports **SystemRDL**
  - Register Description Language
  - Top-level file to generate
- Rapid prototyping of SoCs
  - Quick composition of IP blocks into full systems
- Open-source: SoCMake



SOCRATES – HW input files



SOCRATES – SoCMake outputs

SOCRATES IP LIBRARY
UART, Ibex, ...

USER IP LIBRARY
my_ip, your_ip, our_ip

USER SoC

SoCMake

1. Generation
- SystemVerilog
  - TMR RTL
  - Register file
  - Top module
- SoC HAL (SW)
- Documentation

2. Compilation
- HW & SW

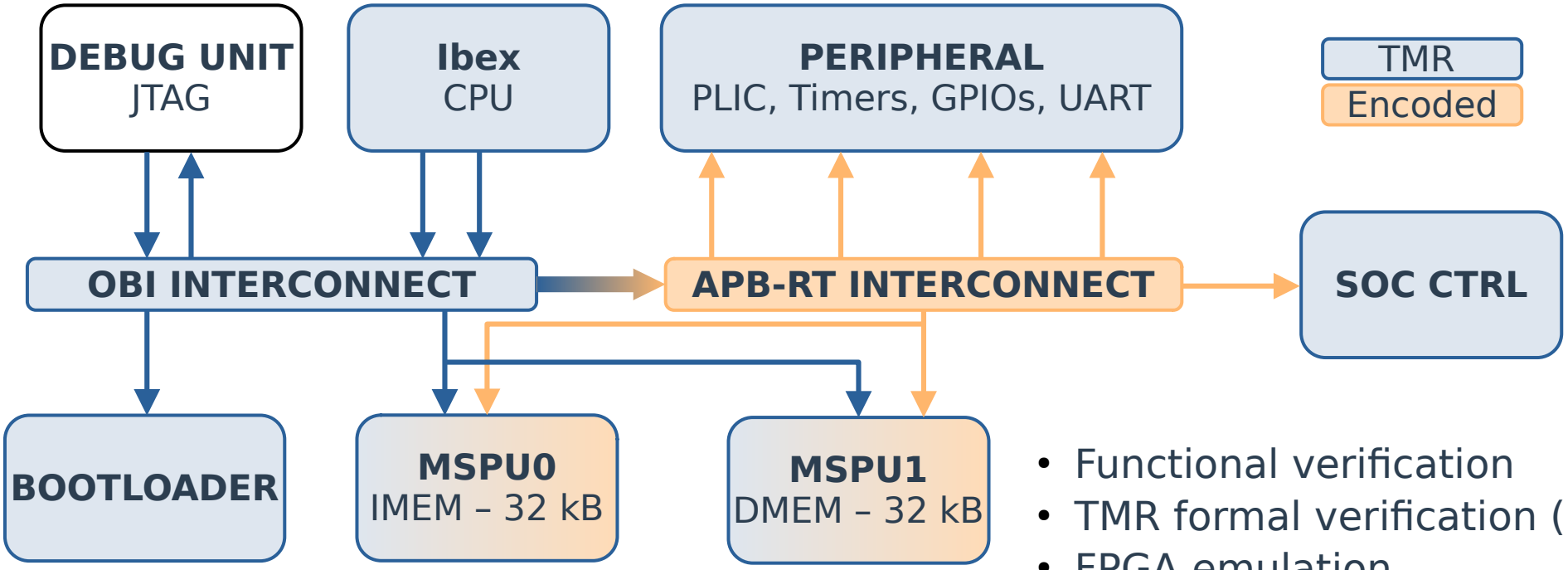
3. Verification
$ make check (-j 8)

```
Test project /home/bdenking/CERN/projects/SOCRATES/SoC_designs/triglav_li
    Start 2: coremark
    Start 6: helloworld_cpp
    Start 3: gpios_blink
    Start 5: helloworld
    Start 4: gpios_test
    Start 7: timer_intrpt
    Start 1: assembly
1/7 Test #1: assembly .......................   Passed    0.08 sec
2/7 Test #7: timer_intrpt ...................   Passed    0.32 sec
3/7 Test #4: gpios_test .....................   Passed    0.32 sec
4/7 Test #5: helloworld .....................   Passed   48.23 sec
5/7 Test #3: gpios_blink ....................   Passed   50.58 sec
6/7 Test #6: helloworld_cpp .................   Passed   60.44 sec
7/7 Test #2: coremark .......................   Passed  109.22 sec

100% tests passed, 0 tests failed out of 7

Total Test time (real) = 109.23 sec
[100%] Built target check
```

TriglaV – Rad-hard demonstrator SoC

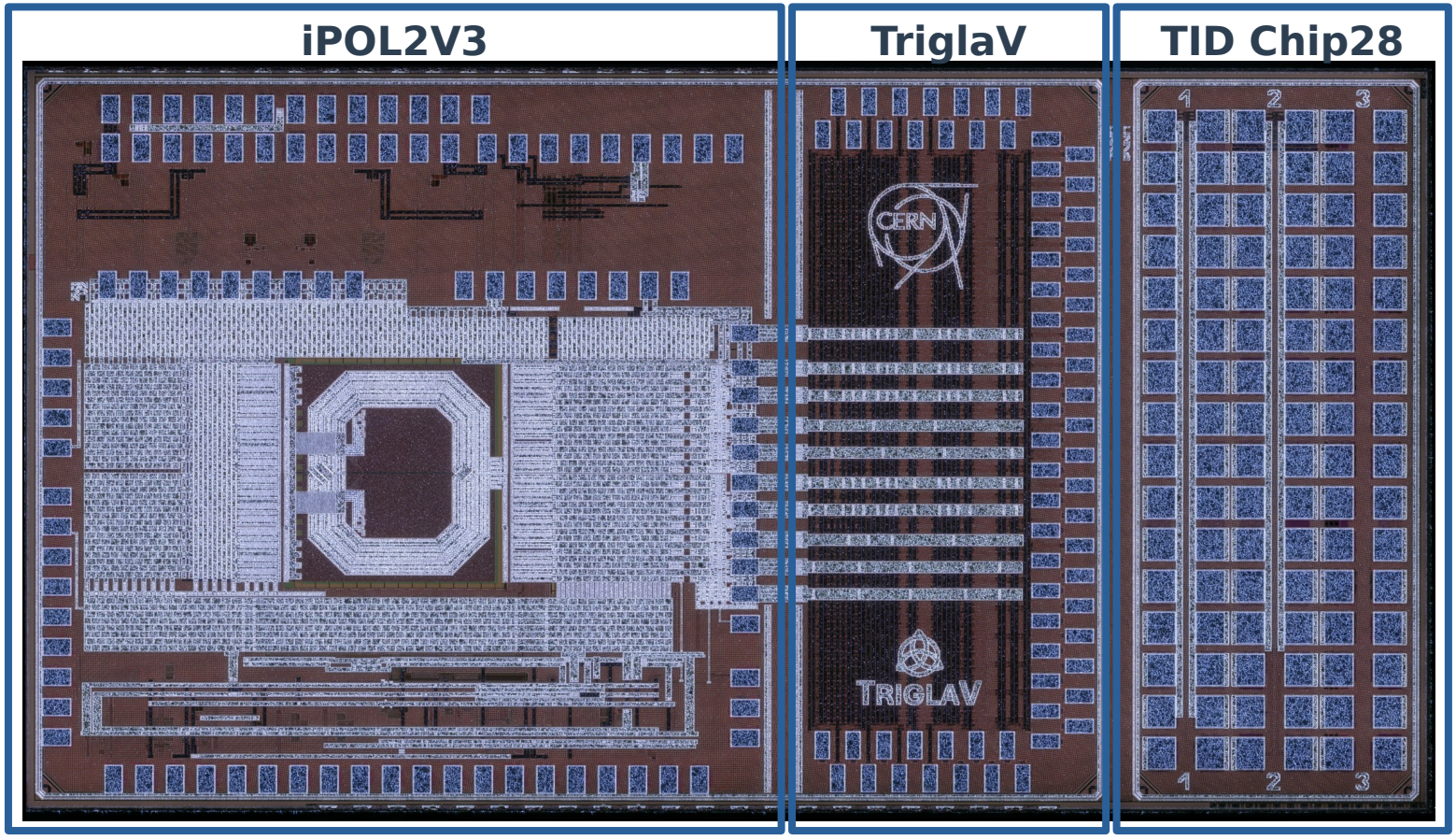
- **Goals**
  - Programmable controller for HEP experiments
  - Demonstrate (and develop) SOCRATES
- **Radiation scenario**
  - Controller for pixel read-out ASIC
    - Fully triplicated (logic) or encoded signals (memories)
- **Implementation**
  - 28nm bulk CMOS (MPW) submitted end of November 2024

TriglaV – Block diagram

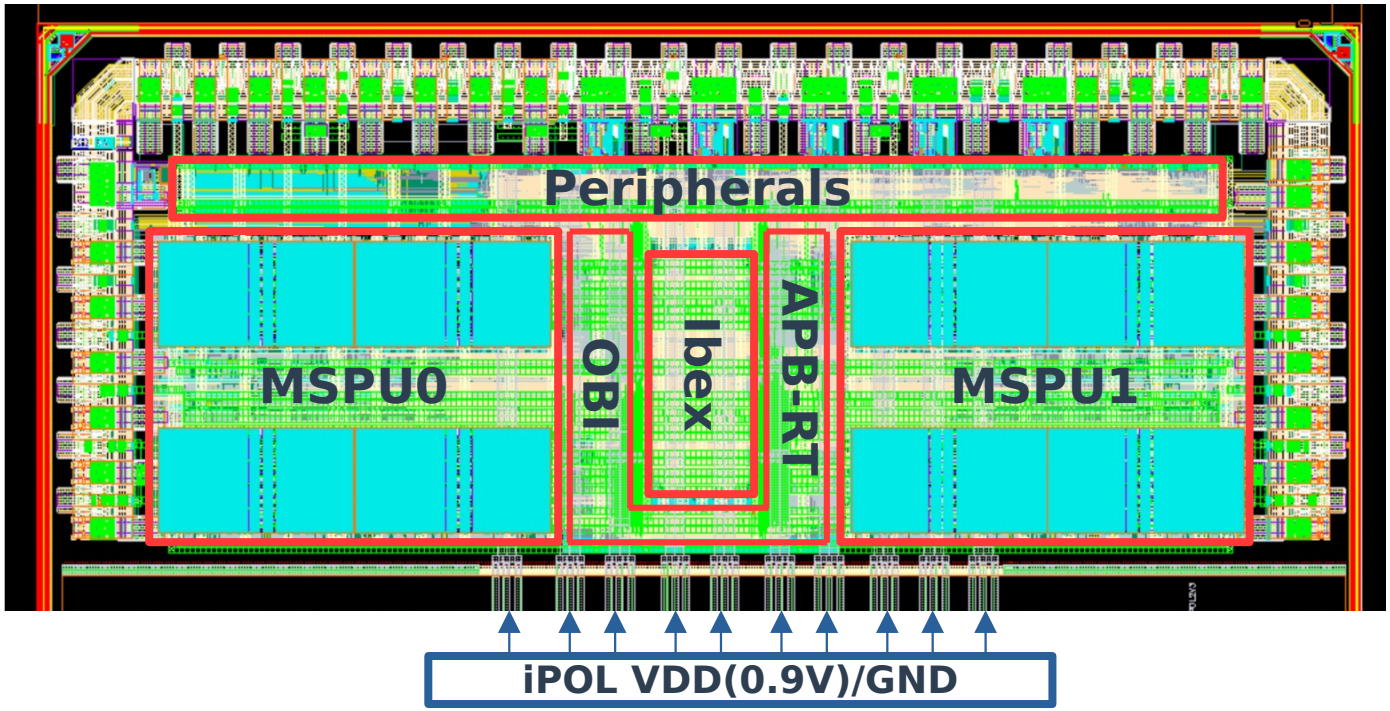


- Functional verification
- TMR formal verification (Ibex)
- FPGA emulation
- Error injection

MPW submission



TriglaV layout



- **Cells**: 12T (LVT,SVT,UHVT)
  - *Ibex 7T*
- **Clock**: 250 MHz
- **Size**: ~1x2 mm^2
- **VDD**
  - Core: 0.9V
  - I/Os: 1.2V
  - Diff I/Os: 0.4±0.2V
- **Power modes**:
  - iPOL2V3 (1 domain)
  - Standalone (4 domains)
    - Ibex (CPU)
    - MSPU (2x)
    - Everything else

TriglaV I/O pads

- **Control**
  - Clock (diff) and asynchronous reset (2)
  - Boot mode (UART, I2C, JTAG) (2)
    - Debug unit enable (non-TMR block)
  - Ibex TMR clock selection (2)
- **Interfaces**
  - UART (2), I2C slave (to OBI master) (2), JTAG (5), GPIOs (8)
- **Testing**
  - Alive (2)
  - Hash (diff) (5) → gold reference
  - Exit valid and value (2)

CERN 28nm IP library:
- RadTol I/O pad (Sofics)
- SLVS (differential) I/O pad

Testing

- **Chip booted < 1 day**
  - Everything works, but...

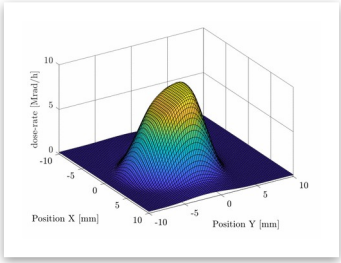
```
Boot Complete
>>> Received: Hello world from Triglav!
```

- **Radiation hardness validation campaign!**
  - Total ionising dose (TID)
  - Single-event effect (SEE)
    - Single-event upsets (SEUs)
    - Single-event transients (SETs)

Radiation Hardness Validation: TID

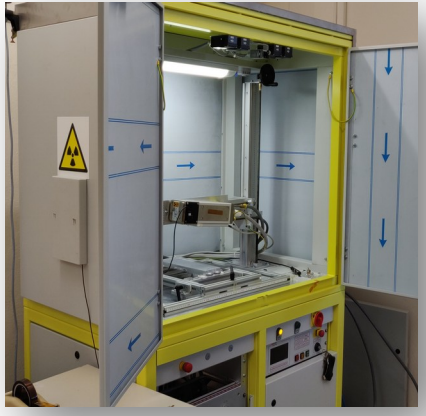
- **CERN X-Ray Irradiation Facility**
  - In-house AsteriX and ObeliX machines
  - Technology and ASIC designs characterization
  - Calibrated X-ray beam to induce precise rate of TID
  - Years of accumulated dose simulated within days

X-Ray Beam Profile

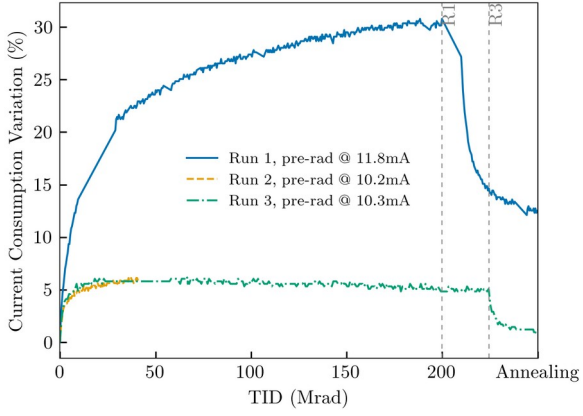


AsteriX

ObeliX



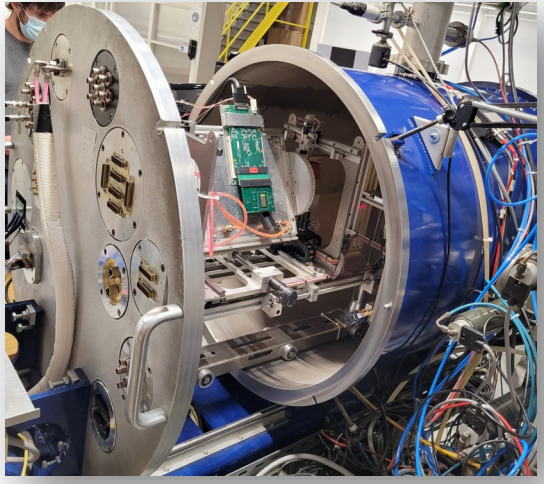
Measurement example:
Leakage current variation over TID

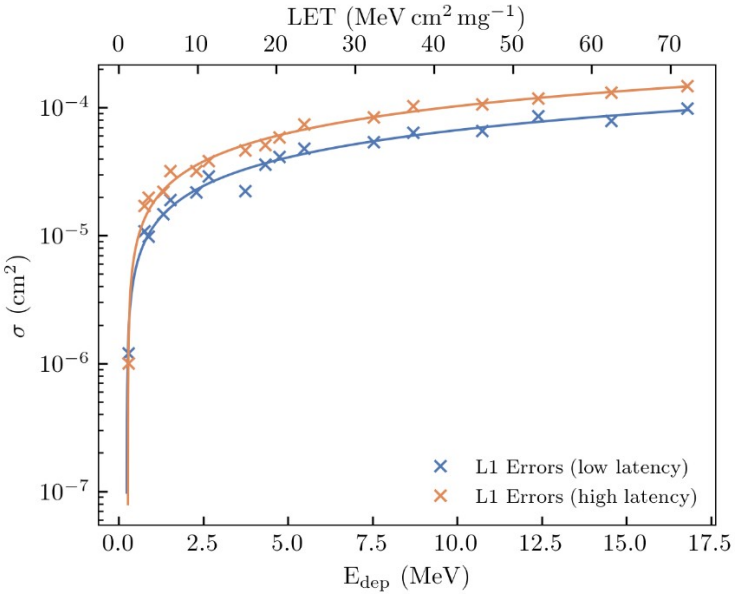


Radiation Hardness Validation: SEE

- **SEE Characterization requires dedicated accelerator facilities**
  - Heavy Ion Facility (HIF) at UCLouvain (Louvain-la-Neuve, BE)
  - Proton irradiation facilities
    - CERN (CH), TRIUMF (Vancouver, CA), PSI (CH)

HIF vacuum chamber, UCLouvain

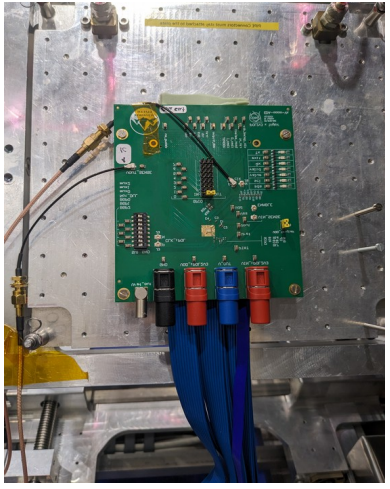


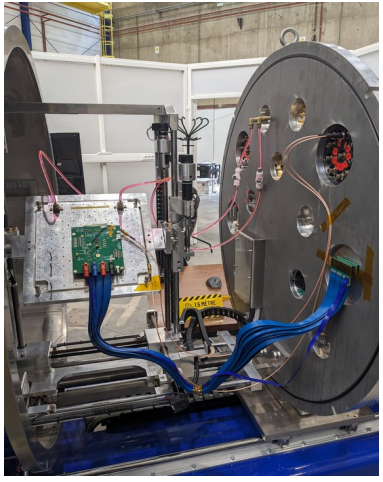


Radiation Hardness Validatino: TriglaV

- **Irradiation tests**
  - HIF – UCL (10h)
  - Laser testing – KU Leuven (1 week)
  - HIF – UCL (12h)
  - Laser testing – CERN (to be started)

Critical failures under investigation





HIF - UCL

Future work

- **TriglaV failure investigation**
  - Technology? Design?
- **RISCV core integration**
  - Picopix pixel readout chip (LHCb experiment)
- **SOCRATES V1 release**
  - SoCMake, plugins, …
- **Rad-hard microcontroller**
  - Sensor monitoring close to the beam

Questions

Thank you!

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